

1. (amended) An integrated circuit structure, comprising:

a capacitive electrode proximate to a sensing surface on which an object is selectively placed,  
the capacitive electrode forming a capacitor with the object when the object is placed on the sensing  
surface;

A5 a dielectric underlying the capacitive electrode; and

an active region underlying the dielectric,

wherein the capacitive electrode and all conductive regions between the capacitive electrode  
and the active region are formed of a conductive material having a hardness greater than a hardness  
of aluminum.

2. (unchanged) The integrated circuit structure of claim 1, wherein the capacitive electrode and each  
conductive region between the capacitive electrode and the active region are formed of a conductive  
material having a hardness at least as great as a hardness of the dielectric.

1 3. (amended) The integrated circuit structure of claim 1, further comprising:

2 a passivation layer over the capacitive electrode, the passivation layer forming the sensing  
3 surface,

4 wherein the capacitive electrode and all conductive regions between the capacitive electrode  
5 and the active region are formed of a conductive material having a hardness at least as great as a  
hardness of the passivation layer.

1 4. (amended) The integrated circuit structure of claim 1, wherein the capacitive electrode and all  
2 conductive regions between the capacitive electrode and the active region are formed of tungsten.

1 5. (unchanged) The integrated circuit structure of claim 4, further comprising:

2 a tungsten via beneath the capacitive electrode.

1 6. (unchanged) The integrated circuit structure of claim 5, further comprising:

2 a tungsten interconnect beneath the via.

1 7. (unchanged) The integrated circuit structure of claim 6, further comprising:

2 a tungsten contact between the interconnect and the active region.

1 8. (unchanged) The integrated circuit structure of claim 7, wherein the active region is a gate  
2 electrode.

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1 9. (amended) An integrated circuit structure, comprising:

2 *A7* an active region;

3 a dielectric overlying the active region and having a contact opening therethrough;

4 a tungsten contact within the contact opening;

5 a tungsten metal region overlying the contact and a portion of the dielectric;

6 an interlevel dielectric overlying the tungsten metal region and the dielectric and having an  
7 opening therethrough;

8 a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel  
9 dielectric, wherein the capacitive electrode is proximate to a sensing surface on which an object is  
10 selectively placed, the capacitive electrode forming a capacitor with the object when the object is  
11 place on the sensing surface and is electrically connected to the active region by the contact, the  
12 metal region, and the via.

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1 14. (amended) A method of forming a scratch resistant integrated circuit structure, comprising:

2 forming an active region;

3 forming a dielectric overlying the active region; and

4 forming a capacitive electrode overlying the dielectric proximate to a sensing surface on  
5 which an object is selectively placed, the capacitive electrode forming a capacitor with the object  
6 when the object is placed on the sensing surface, wherein the capacitive electrode and each  
7 conductive region between the capacitive electrode and the active region are formed of a conductive  
8 material having a hardness greater than a hardness of aluminum.

1 15. (unchanged) The method of claim 14, wherein the capacitive electrode and each conductive  
2 region between the capacitive electrode and the active region are formed of a conductive material  
3 having a hardness at least as great as a hardness of the dielectric.

electro

diel

active

1 16. (amended) The method of claim 14, further comprising:

2 forming a passivation layer over the capacitive electrode, the passivation layer forming the  
3 sensing surface,

AS 4 wherein the capacitive electrode and all conductive regions between the capacitive electrode  
5 and the active region are formed of a conductive material having a hardness at least as great as a  
6 hardness of the passivation layer.

1 17. (amended) The method of claim 14, wherein the capacitive electrode and all conductive regions  
2 between the capacitive electrode and the active region are formed of tungsten.

1 18. (unchanged) The method of claim 17, further comprising:

2 forming a tungsten via beneath the capacitive electrode.

1 19. (unchanged) The method of claim 18, further comprising:

2 forming a tungsten interconnect beneath the via.

1 20. (unchanged) The method of claim 19, further comprising:

2 forming a tungsten contact between the interconnect and the active region.

1 21. (unchanged) The method of claim 20, wherein the active region is a gate electrode.

1 22. (amended) A method of forming an integrated circuit structure, comprising:

2 forming an active region;

3 forming a dielectric overlying the active region and having a contact opening therethrough;

4 forming a tungsten contact within the contact opening;

5 forming a tungsten metal region overlying the contact and a portion of the dielectric;

6 forming an interlevel dielectric overlying the tungsten metal region and the dielectric and  
7 having an opening therethrough;

8 forming a tungsten via within the opening through the interlevel dielectric; and

9 forming a tungsten capacitive electrode overlying the tungsten via and a portion of the  
10 interlevel dielectric, wherein the capacitive electrode is proximate to a sensing surface on which an  
11 object is selectively placed, the capacitive electrode forming a capacitor with the object when the  
12 object is placed on the sensing surface and is electrically connected to the active region by the  
13 contact, the metal region, and the via.

1 23. (unchanged) The method of claim 22, further comprising:

2 forming an oxide over the capacitive electrode and the interlevel dielectric adjacent the  
3 capacitive electrode;

4 forming a passivation layer including a silicon nitride layer and a silicon carbide layer over  
5 the oxide; and

6 forming tungsten ESD protection within the passivation layer.

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1 24. (amended) A method of forming a scratch resistant integrated circuit structure, comprising:

2 forming a plurality of active regions;

3 forming a dielectric over the plurality active regions; and

4 *Amended* forming an array of capacitive electrodes overlying the dielectric proximate to a sensing

5 surface on which an object is selectively placed, the capacitive electrodes each forming a capacitor

6 with the object when the object is placed on the sensing surface and wherein the capacitive

7 electrodes are each formed of a conductive material having a hardness at least as great as a hardness

8 of the dielectric.

1 25. (amended) The method of claim 24, wherein the step of forming an array of capacitive  
2 electrodes overlying the dielectric of a conductive material having a hardness at least as great as a  
3 hardness of the dielectric further comprises:

*Amended*  
4 forming the array of capacitive electrodes of a conductive material having a hardness at least  
5 as great as a hardness of a passivation layer overlying the array of conductive electrodes and forming  
6 the sensing surface.

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1 26. (unchanged) The method of claim 24, wherein the step of forming an array of capacitive  
2 electrodes overlying the dielectric of a conductive material having a hardness at least as great as a  
3 hardness of the dielectric further comprises:

4 forming the array of capacitive electrodes of tungsten.

1 27. (unchanged) The method of claim 24, further comprising:

2 forming each metallization region between the array of capacitive electrodes and the plurality  
3 of active regions of a conductive material having a hardness at least as great as the hardness of the  
4 dielectric.